Reg.No. _____

Karunya UNIVERSITY

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – Nov/Dec – 2016

Code : 14EC3022

Sub. Name : VLSI TECHNOLOGY

Semester : 2016-17 ODD

Duration : 3hrs

Max. marks : 100

ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)

Q. No.	Sub Div.	Questions	Course Outcome	Marks
1.	a.	Explain in detail about the method of depositing a thin layer over a substrate using molecular beam epitaxy.		**20**
		(OR)		
2.	a.	With the help of schematics explain the silicon Shaping operations.		**10**
	b.	What are the processing considerations used for silicon wafer preparation?		**10**
3.	a.	What are the kinetics for thin oxide growth?		**10**
	b.	Explain about the oxide properties in detail.		**10**
		(OR)		
4.	a.	Explain in detail about the methods of E-beam lithography technique with schematic representation.		**10**
	b.	Discuss in detail about DC plasma excitation and A.C plasma excitation		**10**
5.	a.	Explain in detail about the methods of Optical lithography technique with schematic representation.		**10**
	b.	What is Plasma Etching? Write about the properties of Plasma Etching in detail.		**10**
		(OR)		
6.	a.	With the help of equations explain the techniques used for Silicon dioxide and Silicon Nitride deposition.		**20**
7.	a.	Explain the Monte Carlo and the Boltzmann transport equation methods of simulating ion implantation in solids with necessary diagrams and equations.		**20**
		(OR)		
8.	a.	Discuss the diffusion model and silicon oxidation model with necessary mathematical equations.		**20**
		Compulsory:		
9.	a.	Explain NMOS IC technology process in detail.		**10**
	b.	Explain the VLSI assembly technologies in detail.		**10**

ALL THE BEST